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EXAMINER

NADAV, ORI

ART UNIT PAPER NUMBER

2811

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/550,405	IO, EIJI	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 January 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 and 20-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 20-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 April 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: |

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DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides, as recited in claims 1 and 6, a device comprising two first drain and source diffusion layers, as recited in claims 1 and 6, and only one sidewall offset extending along a lateral surface of a gate oxide film, as recited in claims 20 and 22, and heavily doped second source and drain regions being aligned with at least one sidewall covering, as recited in claims 1 and 6, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

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Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-11 and 20-23 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. Figure 4 depicts first drain and source diffusion layers surrounding the bottom and left side of the second drain and source diffusion layers, wherein the STI region abuts the right side of the second drain and source diffusion layers. There is no support for first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides, as recited in claims 1 and 6.

5. Figure 3 depicts two first drain and source diffusion layers and two sidewall offsets extending along a lateral surface of a gate oxide film. Figure 4 depicts one of first drain and source diffusion layers and one sidewall offset extending along a lateral surface of a gate oxide film. There is no support for two first drain and source diffusion

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layers, as recited in claims 1 and 6, and only one sidewall offset extending along a lateral surface of a gate oxide film, as recited in claims 20 and 22.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-11 and 20-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitation of a sidewall offset extending along a lateral surface of a gate oxide film by an amount that is greater than a vertical thickness of the lateral surface of the sidewall, as recited in claims 1 and 6, is unclear as to which thickness is the "vertical thickness", and what is a vertical thickness of a surface (since surface does not have a thickness).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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9. Claims 1, 3-6, 9-11, 20 and 22, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez (5,439,835) in view of Cheng et al. (5,545,575).

Regarding claims 1, 3, 5, 6, 9 and 11, Gonzalez teaches in figure 9 and related text a semiconductor device comprising a memory cell formed on a semiconductor substrate 12, an insulating layer 13 defining device regions, a gate region 16, heavily doped second source and drain regions 23 (figure 2) around the gate electrode and aligned with at least one sidewall covering, at least one sidewall 41 (figure 4) covering the gate electrode and having a sidewall offset extending outwardly of the gate electrode along a horizontal surface of the substrate above only one of the second source and drain regions and along a lateral surface of a gate oxide by an amount that is greater than a vertical thickness of the lateral surface of the sidewall, low resistive wiring layers 92, 51 (figure 5) formed at surfaces of the source and drain layers being located outwardly beyond a peripheral edge of the sidewall offset, at least one of the source and drain region layers extending towards the gate electrode beyond an edge of the sidewall offset.

Gonzalez does not teach first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides.

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Cheng et al. teach in figure 7 first drain and source diffusion layers 43, 44 surrounding second drain and source diffusion layers 57, 58 on at least a bottom and four lateral sides.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides, as taught by Cheng et al., in Gonzalez's device, in order to improve the device characteristics by forming LDD regions in the device.

Regarding claims 4 and 10, Cheng et al. teach in figure 7 second diffusion layers 43, 44 of lower impurity concentration than that of the source and drain regions 57, 58 (column 4, lines 24-26 and column 6, lines 2-4) formed below the source and drain regions.

Regarding claim 6, Cheng et al. teach in figure 7 silicide wiring layers 64 formed at surfaces and in the source and drain layers located outwardly beyond a peripheral edge of the sidewall offset. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form silicide wiring layers at surfaces and in the source and drain layers located outwardly beyond a peripheral edge of the

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sidewall offset in Gonzalez's device in order to reduce the contact resistance of the device.

Regarding claims 20 and 22 Gonzalez teaches in figure 9 only one sidewall offset.

10. Claim 7, insofar as in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez and Cheng et al., as applied to claim 6 above, and further in view of Kunishima et al. (5,316,977).

Gonzalez and Cheng et al. teach substantially the entire claimed structure, as applied to claim 1 above, except a silicide layer comprising titanium silicide.

Kunishima et al. teach in figure 5C a silicide layer 21 comprising titanium silicide.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a titanium silicide in Gonzalez and Cheng et al.'s device, because titanium silicide is a conventional silicide material, of which official notice is taken.

11. Claims 1-4, 6, 8-10, 21 and 23, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al.

Cheng et al. teach in figure 15 a semiconductor device comprising a semiconductor substrate 11, an insulating layer 19 defining device regions, a gate region 28 and the

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insulating layer defining lightly doped first drain or source diffusion layers 77', 78', heavily doped second source and drain regions 82, 84 around the gate electrode and aligned with at least one sidewall covering, with the first drain and source diffusion layers 77', 78' surrounding the second drain or source diffusion layers 82, 84 on at least a bottom and four lateral sides, a sidewall 66 covering the gate electrode and having a sidewall offset extending outwardly of the gate electrode along a horizontal surface of the substrate in both regions above the second source and drain regions and along a lateral surface of a gate oxide by an amount that is greater than a vertical thickness of the lateral surface of the sidewall, silicide wiring layers 64 formed at surfaces of the source and drain layers being located outwardly beyond a peripheral edge of the sidewall offset, at least one of the source and drain region layers extending towards the gate electrode beyond an edge of the sidewall offset, and second diffusion layers 43, 44 of lower impurity concentration than that of the source and drain regions (column 4, lines 24-26 and column 6, lines 2-4) formed below and surrounding the source and drain layers.

Cheng et al. do not teach in the embodiment of figure 15 first drain and source diffusion layers. Cheng et al. teach in the embodiment of figure 7 first drain and source diffusion layers 43, 44 surrounding second drain and source diffusion layers 57, 58 on at least a bottom and four lateral sides.

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It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides in Cheng et al.'s device, in order to improve the device characteristics by forming LDD regions in the device.

Regarding claims 21 and 23, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to cover entirely the gate electrode of Cheng et al.'s device with the sidewall in order to provide better protection for the gate in an application which does not require external connection to the gate.

12. Claims 5, 7, 11, 21 and 23, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al., as applied to claims 1 and 6 above, and further in view of Kunishima et al.

Cheng et al. teach substantially the entire claimed structure, as applied to claims 1 and 6 above, except a silicide layer comprising titanium silicide.

Kunishima et al. teach in figure 5C a silicide layer 21 comprising titanium silicide.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a titanium silicide in Cheng et al.'s device, because titanium silicide is a conventional silicide material, of which official notice may be taken.

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Regarding claims 5 and 11, Kunishima et al. teach using the semiconductor device as a CMOS device, and it is well known in the art that CMOS devices are used as memory devices.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Cheng et al.'s device as a memory device, because the intended use of a device depends on the requirements of the application in hand. Note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claims 21 and 23, Kunishima et al. teach in figure 5C a sidewall entirely covering the gate electrode. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to cover entirely the gate electrode of Cheng et al.'s device with the sidewall in order to provide better protection for the gate in an application which does not require external connection to the gate.

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Response to Arguments

13. Applicant argues on page 4 that figure 4 supports first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides, as recited in claims 1 and 6.

Figure 4 depicts first drain and source diffusion layers surrounding the bottom and left side of the second drain and source diffusion layers, wherein the STI region abuts the right side of the second drain and source diffusion layers. Therefore, there is no support for first drain and source diffusion layers surrounding the second drain and source diffusion layers on all four lateral sides, as recited in claims 1 and 6.

14. Applicant argues on pages 4-5 that prior art figures 1-2 and figure 4 support a device comprising two first drain and source diffusion layers, as recited in claims 1 and 6, and only one sidewall offset extending along a lateral surface of a gate oxide film, as recited in claims 20 and 22.

Neither prior art figures 1-2, nor figure 4 depict and support a device comprising two first drain and source diffusion layers, as recited in claims 1 and 6, and only one sidewall offset extending along a lateral surface of a gate oxide film, as recited in claims 20 and 22.

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15. Applicant argues that Gonzalez and Cheng et al. do not teach a sidewall offset extending along a lateral surface of a gate oxide by an amount that is greater than a vertical thickness of the sidewall

Figure 15 of Cheng et al. clearly depict a sidewall offset having a vertical edge along a lateral surface of a gate oxide that is further out than the vertical edge of the sidewall along the gate sidewall. Figure 9 of Gonzalez clearly depict a sidewall offset having a vertical edge along a lateral surface of a gate oxide that is further out than the vertical edge of the sidewall along the gate sidewall. Thus, Gonzalez and Cheng et al. teach a sidewall offset extending along a lateral surface of a gate oxide by an amount that is greater than a vertical thickness of the sidewall, as claimed.

16. Applicant argues that Gonzalez does not teach silicide metal lines.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Although Gonzalez does not teach a metal silicide layer comprising titanium silicide, Kunishima et al. is cited to teach a silicide layer comprising titanium silicide.

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Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772**.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

A handwritten signature in black ink, appearing to read "Ori Nadav", is positioned above the printed name and title.

O.N.
March 13, 2003

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800